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LOW POWER COMPARATOR WITH FAST PROPAGATION DELAY

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TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to integrated circuit comparators and, more specifically, to reducing propagation delay in integrated circuit comparators.

BACKGROUND OF THE INVENTION

[0002] As illustrated in the equivalent circuit diagram depicted in FIGURE 5, integrated circuit comparators typically include: a bias system generating a defined current bias to each transistor; an input differential pair--either complementary metal oxide semiconductor (CMOS) or bipolar junction transistors--that, for a given over-drive voltage V(ov)=(V(inp)-V(inn) generate a differential current given by I(ov)=gm*V(ov), where gm is the trans-conductance of the input differential pair at the steady-state operating point V(ov)=0 volts (V); a gain stage node ngain converting the current I(ov) to (in the CMOS case) a voltage gain and having a transition speed depending on the overdrive current I(ov) available, the voltage excursion

required between the high and low levels at the ngain node, and the capacitive load at the ngain node, including any Miller capacitance from the comparator's output stage; and a gain stage assuring a given slew rate at the comparator output out.

[0003] Additional non-ideal effects for most comparators include random and systematic offset of the input differential pair, the common mode rejection ratio of the input differential pair, and power supply rejection and propagation delay dependence on the power supply voltage. For example, a comparator's propagation delay will typically be related to the applied overdrive voltage V(ov), with a lower overdrive voltage resulting in a longer propagation delay (but consuming greater power).

[0004] Some techniques currently proposed or employed to reduce the comparator's propagation delay include reducing the capacitive loading of the comparator's ngain node, increasing the transconductance gm of the input differential pair by, for instance, increasing the bias current applied to that input differential pair, and reducing the voltage excursion of the ngain node to a minimum.

[0005] There is, therefore, a need in the art for alternatives for reducing an integrated circuit

comparator's propagation delay while limiting power consumption by the comparator.

SUMMARY OF THE INVENTION

[0006] To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide, for use in an integrated circuit comparator, a pulsed rather than continuous bias current applied, in at least a fast comparator configuration, to a current source within a comparator's input gain stage driven by a current proportional to the transconductance of a differential pair of input transistors receiving voltage signals to be compared is pulsed rather than continuous. The pulse with of the bias current is small relative to the system clock, but has a large current magnitude allowing the comparator to quickly respond to applied voltages, but without unacceptable increase in current and power consumption. A voltage limiter and hysteresis circuit minimize spurious currents when the bias current pulse is inactive. The bias current pulse and sampling of the comparator occur in predefined relation to the system clock.

[0007] The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows.

Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art will appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Those skilled in the art will also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

[0008] Before undertaking the DETAILED DESCRIPTION OF THE INVENTION below, it may be advantageous to set forth definitions of certain words or phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or" is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one

operation, whether such a device is implemented in hardware, firmware, software or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, and those of ordinary skill in the art will understand that such definitions apply in many, if not most, instances to prior as well as future uses of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, wherein like numbers designate like objects, and in which:

[0010] FIGURE 1 depicts an equivalent circuit diagram for a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention;

[0011] FIGURES 2A-2C are timing diagrams illustrating operation of a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention;

[0012] FIGURE 3 is a block diagram of a low power integrated circuit pulse generator and comparator according to one embodiment of the present invention;

[0013] FIGURES 4A and 4B are circuit diagrams for a pulse generator and a comparator according to one embodiment of the present invention; and

[0014] FIGURE 5 is an equivalent circuit diagram of a typical integrated circuit comparator.

DETAILED DESCRIPTION OF THE INVENTION

[0015] FIGURES 1 through 4B, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any suitably arranged device.

[0016] FIGURE 1 depicts an equivalent circuit diagram for a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention. Comparator circuit 100 is formed within an integrated circuit device and includes a differential input pair V(inp) and V(inn) producing a pulsed trans-conductance gm received as an input by a first gain stage 101. The pulse input changes the bias current Ibias from the current source I1, changing the bias current of the whole comparator 100.

[0017] The first gain stage 101 includes an output resistance go and output capacitance (including Miller capacitance) Cp in parallel with the current source I1. Connected to the output of the first gain stage 101 is a

voltage limiter 102 and a built-in hysteresis circuit 103 including a current source I2 driven by a hysteresis current signal Ihys that is switched into and out of parallel connection with the first gain stage 101 at the output of the first gain stage 101 based on the comparator's output voltage out. Connected between the output of the first gain stage 101 (and to hysteresis circuit 103) is a second gain stage 104 including a current source I3 driven by a gain signal A2*ngain.

[0018] In the exemplary embodiment of the invention depicted in FIGURE 1, the second gain stage 104 changes gain A2*ngain based on the pulsed input. However, in an optimized version of the circuit, the gain of the second gain stage 104 may remain constant (i.e., simply A2) since the transition delay for the second gain stage 104 is negligible with respect to the transition delay of the first gain stage 101.

[0019] The comparator 100 of the present invention employs the techniques described above for optimizing propagation delay within a given current budget defined by power consumption constraints, such as minimizing capacitive loading of the node ngain and keeping the voltage excursion of the ngain node to a minimum.

[0020] In addition, comparator 100 utilizes an input voltage that is steady at a defined time t1 relative to the system clock. An input signal pulse arrives at time t1 with a duration of pulse_w. While the input signal pulse is active, the internal bias current of the comparator increases by a factor n_speed=5*7=35 times; when the pulse signal becomes inactive, the internal bias current returns to the nominal level.

[0021] The output voltage out of the comparator is sampled at a time t2, where t2−t1>0 and t2−t1 is precisely defined, with the sampling period of duration t_sample commencing at t2. The small internal hysteresis circuit 103 reduces false triggering at the output out during the pulse_w period.

[0022] Comparator 100 is capable of operating within a large range of bias current values without inverting the output voltage out. That is, given a nominal bias current ibais, comparator 100 is able to operate with a bias current range between ibias/7 to 5*ibias.

[0023] In an i_power_low_speed mode (or "low power comparator" configuration), the quiescent current of the amplifier (first gain stage 101) is driven with a constant bias current of ibias/6, so that comparator 100 has low power consumption but a long propagation delay slow_prop.

In an i_power_high_speed mode (or "fast comparator" configuration), the quiescent current of the amplifier is driven with a constant bias current of 5*ibias, such that comparator 100 has higher power consumption but a faster propagation delay fast_prop.

[0024] FIGURES 2A through 2C are timing diagrams illustrating operation of a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention. FIGURE 2A illustrates operation of comparator 100 in the low power comparator configuration. When the applied overdrive voltage V(ov) changes from +10 milli-Volts (mV) to 0, the voltage at node ngain changes slowly and the output voltage does not change (i.e., remains at 3 V or a logical "high"). Once the applied overdrive voltage V(ov) changes to −10 mV, the output voltage out toggles (i.e., changes to −1.0 V or a logical "low").

[0025] At room temperature with an integrated circuit comparator fabricated with typical processes and a V(inn) of 1.5 V, the worst case propagation delay for an overdrive voltage V(ov) varying between ±10 mV, a worst case output propagation delay is approximately 5 microseconds (μs). Moreover, the propagation delay increases if the overdrive voltage V(ov) decreases. If V(ov)=±3 mV, the propagation

delay increases to 30 μs. Comparator 100 will not toggle in the low power comparator configuration for |V(ov)|<2 mV.

[0026] FIGURE 2B illustrates operation of comparator 100 in the fast comparator configuration, but with a pulsed bias current. With the pulsed bias at a pulse width of 390 nanoseconds (ns), the propagation delay shortens to 0.6 μs for an overdrive voltage V(ov)=±10 mV.

[0027] FIGURE 2C illustrates operation of comparator 100 in the fast comparator configuration with pulsed bias current and an overdrive voltage V(ov)=±2 mV. The system clock employed has a period of 10 μs, giving a bias current pulse to clock period ratio of 390 ns/10 μs or 3.9%. The resulting output propagation delay is 0.8 μs. Aside from some narrow current spikes, the quiescent current ranges from 360 nano-Amps (nA) when the bias current pulse is active to 5 micro-Amps (μA) when the bias current pulse is inactive, with an average quiescent current for the fast comparator configuration of about 545 nA, or only approximately 50% more than the quiescent current of the slow comparator configuration despite an increase of the bias current magnitude from ibias/6 to 5*ibias.

[0028] With respect to the propagation delay performance of the slow comparator configuration, the fast comparator configuration with pulsed bias current takes 50% more

quiescent current but improves propagation delay from 30 μs to 0.8 μs, more than 30 times faster.

[0029] A pulse generator (not shown in FIGURE 1) coupled to the comparator 100 produces the 390 μs bias current pulse. Transistors within comparator 100 are sized for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs. The analog inputs are expected to reach their steady state before the falling edge of the system clock (clk) signal, where the system clock period is 20 μs and the clock duty cycle is 50%. The pulse generator produces a 390 ns wide pulse on every falling edge of the clk signal, and the comparator output out is sampled with the clk signal's rising edge.

[0030] In the present invention, an overcurrent of nearly 5*7 times larger than the bias condition of the "low power" or slow comparator configuration drives the ngain node in the fast comparator bias condition, which helps the ngain node to reach steady state in a shorter time and reduce propagation delay. The comparator's average power consumption in pulsed bias current mode depends on the ration between pulse_w and t_sample. For a small pulse_w/t_sample ratio, the comparator's average power

consumption will be similar to the value of the low power slow comparator configuration's i_power_low_speed.

[0031] In the exemplary embodiment, the comparator's propagation delay will range between values fast_prop/2 and fast_prop, with the resulting comparator having speed similar to the fast comparator configuration but with lower quiescent current. The pulsed bias current comparator with elevated bias current magnitude responds to smaller overdrive voltages V(ov) than the slow comparator configuration. Furthermore, the same principle employed in the present invention may be employed for an operational amplifier to reduce slewing and settling time while keeping a relatively small quiescent power consumption.

[0032] FIGURE 3 is a block diagram of a low power integrated circuit pulse generator and comparator according to one embodiment of the present invention. System 300 includes pulse generator 301, a buffer or inverter 302, and comparator 100. The circuit 300 receives as inputs power supply voltages vss and vdd, a reference voltage vref and an input signal in to be compared to the reference voltage, an enable input enable, a phase signal phase, a bulk bias voltage nbulk, comparator bias current icomp and a signal ibiaspulse selecting pulsed biasing of the comparator 100.

[0033] FIGURES 4A and 4B are, taken together, a circuit diagram for a comparator according to one embodiment of the present invention. The circuit depicted corresponds to comparator 100.

[0034] Although the present invention has been described in detail, those skilled in the art will understand that various changes, substitutions, variations, enhancements, nuances, gradations, lesser forms, alterations, revisions, improvements and knock-offs of the invention disclosed herein may be made without departing from the spirit and scope of the invention in its broadest form.